least two consecutive inverters being configured with common initial conditions so as to produce a distinctive pattern during operation of the first delay line, wherein a level of supply voltage on the supply voltage input affects switching speed of the cascaded inverters;

a second delay line including an input configured to be coupled to a data source, multiple outputs, and a control input;

a comparator including a first input coupled to an output of the first delay line, a second input coupled to a clock, and at least one output, the comparator being configured to provide on the output an error signal between the output of the first delay line and the clock;

a control signal line coupled to the at least one output of the comparator, the supply voltage input of the first delay line, and the control input of the second delay line, the control signal line being configured to provide a control signal, based on the error signal, to the supply voltage input of the first delay line and the control input of the second delay line;

a sampling signal line coupled to, and configured to provide a sampling signal based on, the at least one output of the first delay line; and

a sampling device coupled to the multiple outputs of the second delay line and coupled to the sampling signal line, the sampling device configured to sample the multiple outputs of the second delay line based on a value of the sampling signal.

23. (Previously Presented) The circuit of claim 22 wherein:

the second delay line comprises an odd number of cascaded inverters,

the control input comprises a supply voltage input, and

a level of supply voltage on the supply voltage input of the second delay line affects switching speed of the cascaded inverters of the second delay line.